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Clock parameter tuning with an intelligent adaptive learning to improve performance and power of Multisource Clock Tree Synthesis

Divyarajsinh Vaghela, Jagadeesh Gnanasekaran, Gaurav Bhatia, Raj Dua
INTEL



Problem Statement

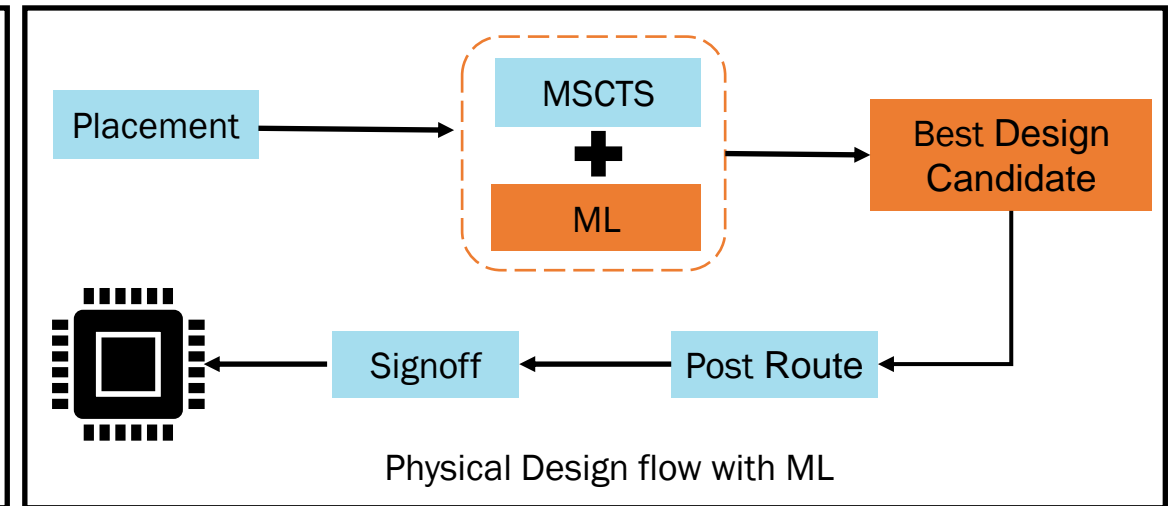
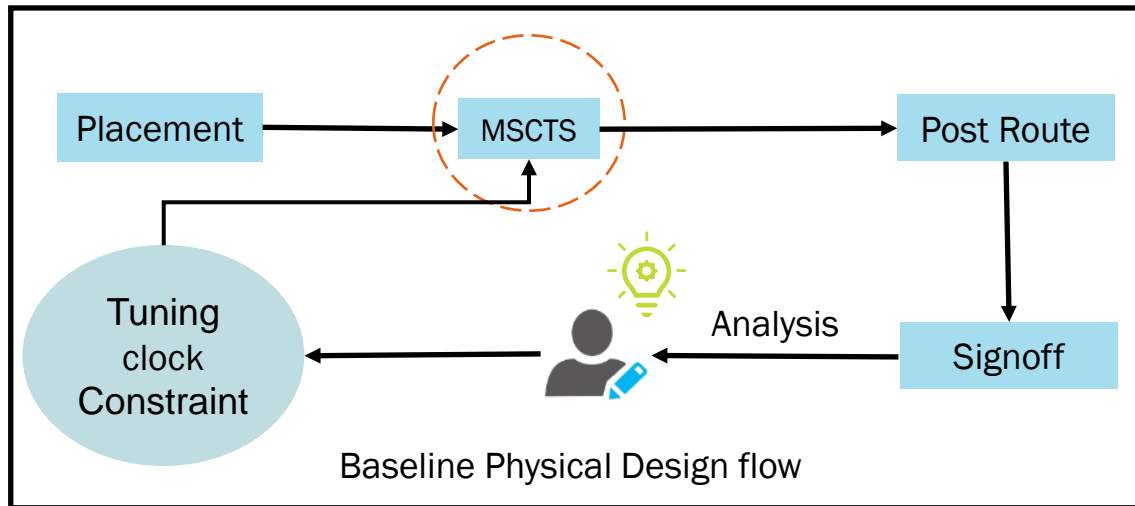
- Clock parameter tuning and optimization of clock networks in lower technology nodes is one of the challenges in Backend design.
- Identifying best recipe that affect timing and some additional parameters that may improve timing cannot be tested in a short amount of time and it is a time-consuming process that requires significant effort from the design engineer.
- Designer need to run multiple experiments by manually changing the design settings
 - Compare Multiple Experimental results.
 - Produce a working recipe of design settings and inputs so that Performance and Power are met.
 - Selection of the right database after comparison of QoR for further steps.

Solution Statement

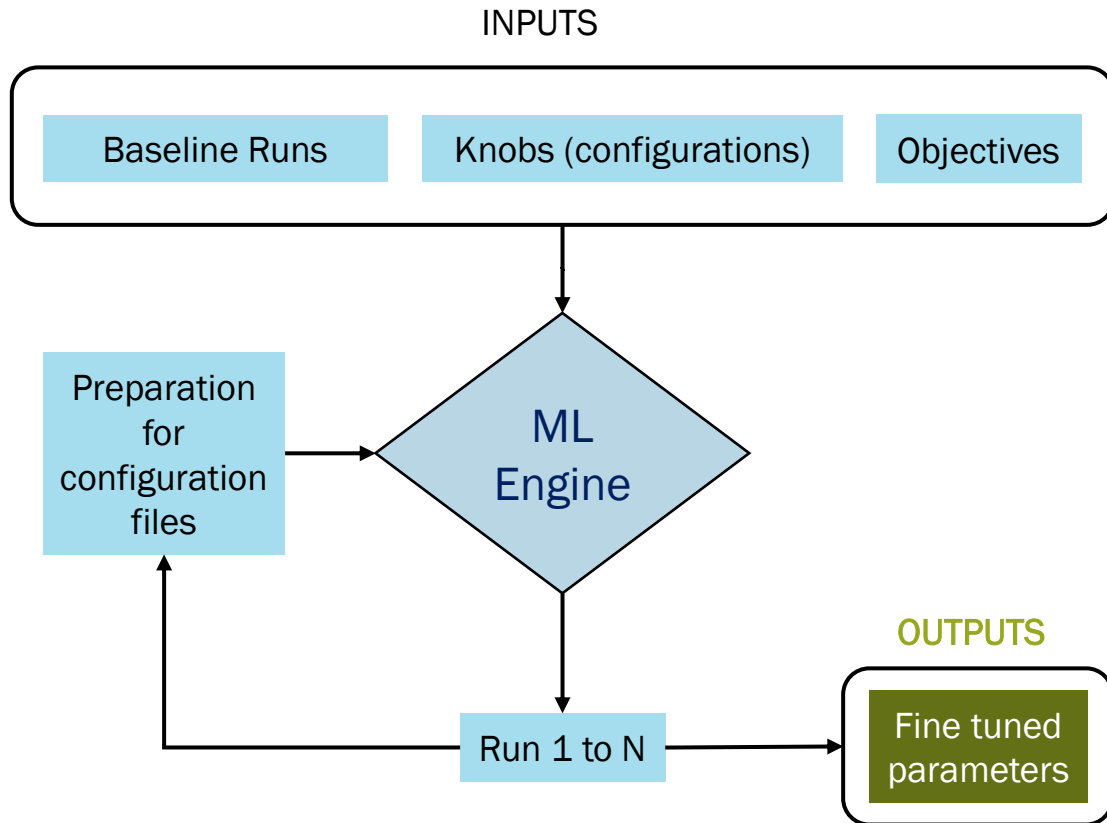
- Motivation to use Adaptive learning engine in Physical Design is to free the engineer from the drudgery of manual search, comparing and learning. Tool capability gives us the best way to sweep multiple parameters in an efficient way to tune recipes to achieve best Power, Performance and Area.
- This approach provides an explanation to the user that justifies its recommendations, decision, or action. The user decides based on the explanation.

Working Model (MSCTS+ML)

- The construction of high quality clock tree is dependent on design constraints such as clock buffer choice, maximum fanout, max net length, target global skew and tool application (app) options for timing and power optimization.
- Right clock tree power and performance targets can be achieved by tuning the design constraints and app options. However, since these parameters can have complex relationship to each, experimenting with different combination of parameter settings manually is difficult and time consuming.
- In this work we utilize machine learning based parameter tuning tool to identify optimal design constraints and app option combinations to build high performance and low power Multisource clock tree (H-tree).



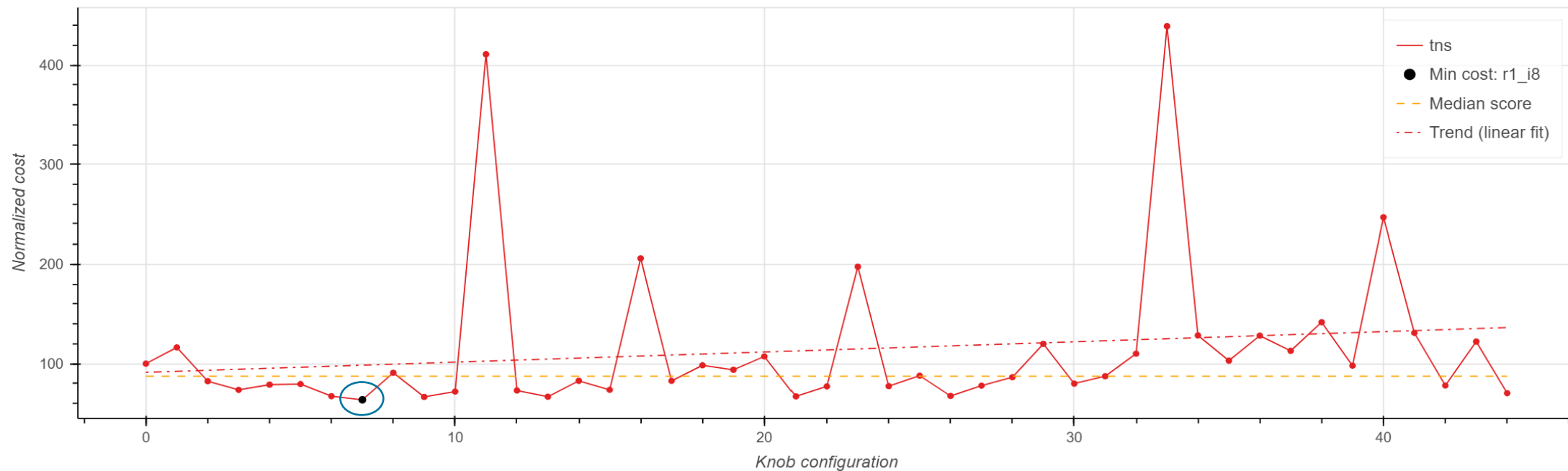
Intelligent Adaptive Learning driven Tool



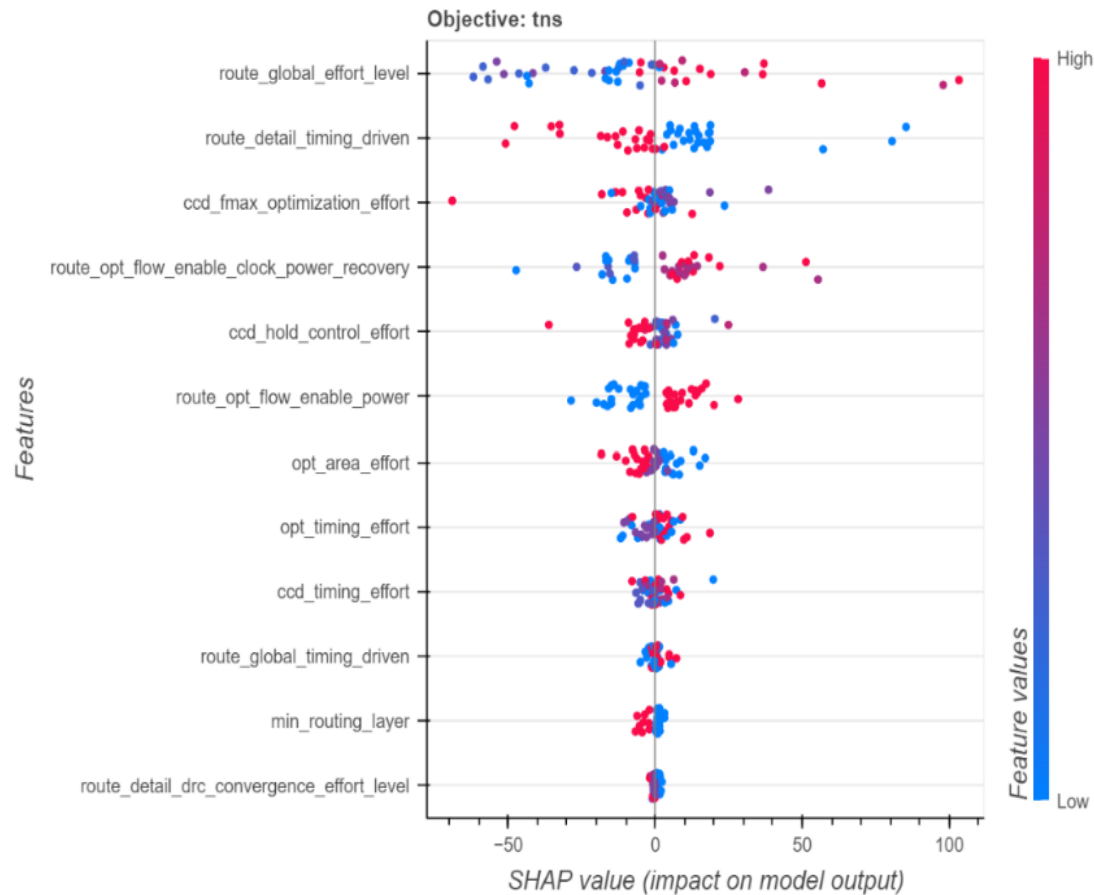
- This tool is an Intel ML (machine learning) approach allowing tool to explore all possibilities within predefined user inputs/objectives/knobs to achieve best QoR.
- Natively supports user defined customized ML algorithm.
- ML engine will take parameters (i.e App options) and measurable objectives (i.e WNS, TNS, Area, Power, Leakage etc) as an input.
- It will perform 1 to N rounds of iteration to get best PPA results by fine tuning parameters.

Intelligent Adaptive Learning driven Tool [cont.]

- The datapoints graph of multiple runs with ML base engine for one of the objectives is shown below.
- Each dot point in graph represents learning-based iteration with fine tuning of parameters to achieve minimum cost of objective.



Intelligent Adaptive Learning driven Tool [cont.]



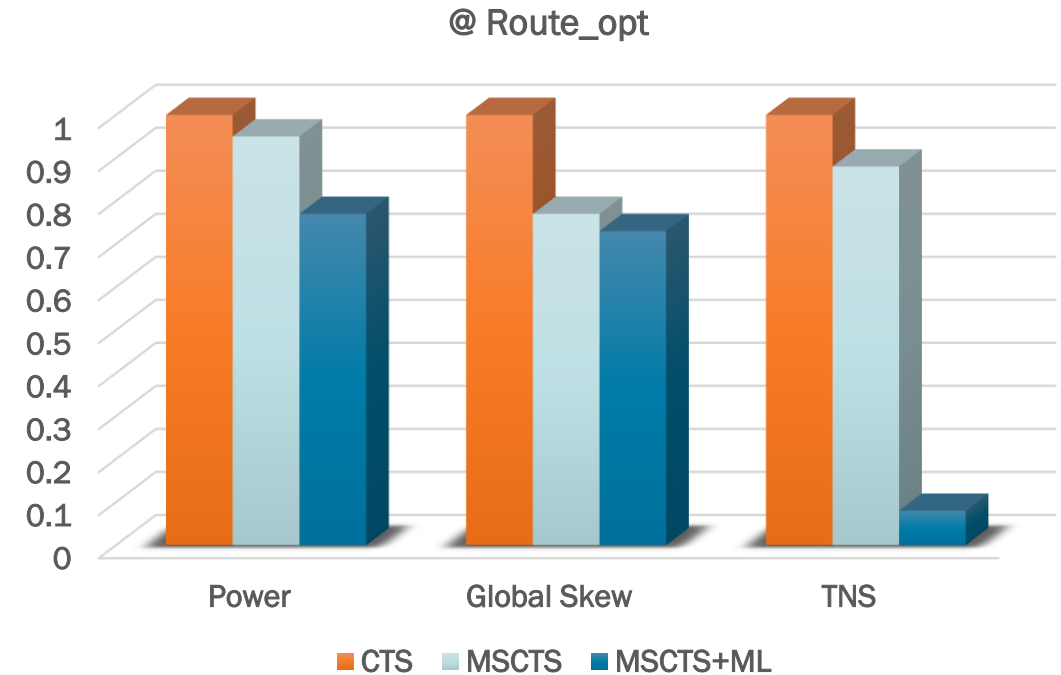
- The figure shows SHAP value of objective.
- Each dot corresponds to an individual configuration in the study.
- Each individual configuration is repeated in every row for every knob.
- The position of the dot on the x-axis is the impact that feature has on the prediction of the objective, i.e. (approximately) on the objective result for this specific configuration.
- SHAP value graph explains which knob (i.e app options) is having maximum contribution to achieve best objective value.
- Lower feature value (indicated in blue dots) is desirable.

Results

- For our experiments, primary tool used for Multisource CTS is from commercial EDA vendor and for parameter tuning is Intel proprietary and objective is set to minimize skew, TNS and Power.
- The parameters that affect skew, TNS and power of the H – Tree based clock tree synthesis is tuned with ML flow and selected parameters are used to complete physical implementation up to route optimization.
- The results for the Machine Learning Based optimization are given below. Power and performance metrics of best parameter tuning outcome for each of the baseline run is shown in below table.

Route_opt QOR (20k sinks)	CTS	MSCTS	MSCTS+ML	Improvement
Max Latency	1	0.96	0.95	5%
Global Skew	1	0.77	0.73	27%
WNS	1	0.75	0.57	43%
TNS	1	0.88	0.08	92%
Power	1	0.95	0.77	23%

Note: Value mentioned in table is normalized value.



Summary

- With the help of Multisource clock tree synthesis (H-tree) and Machine Learning-based parameter adjustment, we can quickly construct high-performance clock networks.
- The outcome indicates, ML-based tuning performed on timing and power metrics produced better results as compared to manually chosen parameters in the baseline run.
- By enhancing the timing and power metrics of clock distribution networks, this method can increase the efficiency and performance of synchronous circuits.